FPGA Design of Self-certified Signature Verification on Koblitz Curves

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Outline

Introduction

- Packet Level Authentication (PLA)[1]
  - Enormous speed requirements!
  - Elliptic curve cryptography because short signatures and fast performance are needed
  - Koblitz curve, NIST K-163, used to maximize speed
  - Self-certified ID based signatures because they are short and computationally less complex

[1] See http://www.tcs.hut.fi/Software/PLA/new/index.shtml

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  - Koblitz curve, NIST K-163, used to maximize speed
  - Self-certified ID based signatures because they are short and computationally less complex
- Development in FPGA technology
  - Growth in resources enables massive parallelization
  - Point multiplication times $< 100\ \mu$s have been reported
- We focus on maximizing operations per second instead of minimizing computation time of a single operation

[1] See http://www.tcs.hut.fi/Software/PLA/new/index.shtml

Koblitz curves

- Koblitz curves have the form

$$E_K : y^2 + xy = x^3 + ax^2 + 1$$

- If $P = (x, y)$ is a point on E_K, then its Frobenius endomorphism, $\phi(P) = (x^2, y^2)$, is also on E_K.
- Very efficient point multiplication
  - Integer presented in τ-adic non-adjacent form (NAF)[2]
  - Point doublings replaced by Frobenius maps
  - Only $m/3$ point additions

[2] Solinas, Des. Codes Cryptogr. 19(2-3), 2000

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A signature is verified by computing:

$$W_A = \text{DECOMPRESS}(r_A - \text{HASH}(ID_A), b_A) - r_A W_D, \text{ and}$$

$$\text{HASH}(\mathcal{M}) = c - [dG + cW_A]_x \pmod{r}$$

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which simplify into the 3-term point multiplication:

$$dG + c(uG) - cr_A W_D = k_1 P_1 + k_2 P_2 + k_3 P_3$$

Point multiplication

$$Q = k_1 P_1 + k_2 P_2 + k_3 P_3$$

- Shamir's trick $\Rightarrow$ 3-term double-and-add algorithm
- 3-term τ-adic joint sparse form[3]

Simplified algorithm

1. Precompute all possible combinations $R_{k_1,k_2,k_3} = k_{1,j}P_1 + k_{2,j}P_2 + k_{3,j}P_3$
2. Perform $\phi(P)$ for all bits
3. If $k_{1,j}, k_{2,j}, k_{3,j} \neq 000$, add R_{k_1,k_2,k_3} to Q using mixed coordinate point addition[a]

[a] Al-Daoud et al. IEEE Tran. Comp. 51(8), 2002

[3] Brumley, ICICS 2006, LNCS 4307

Precomputed points

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- Pairs (R_k, R_{k+1}) are computed so that
  1. $R_k = R_i + R_j$, and
  2. $R_{k+1} = R_i - R_j$
- Unified point addition and subtraction: $(R_k, R_{k+1}) \leftarrow R_i \pm R_j$

Unified point addition and subtraction

Point addition

$(x_3, y_3) = (x_1, y_1) + (x_2, y_2)$

$$\lambda = \frac{y_1 + y_2}{x_1 + x_2}$$
$$x_3 = \lambda^2 + \lambda + x_1 + x_2 + a$$
$$y_3 = \lambda(x_1 + x_3) + x_3 + y_1$$

Point subtraction

$(x_4, y_4) = (x_1, y_1) - (x_2, y_2)$

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- Inversion is the same[4]

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- Inversion is the same[4]
- Some additions can be saved by rearranging operations
- Total cost reduces from $2I + 4M + 2S + 17A$ to $I + 4M + 2S + 14A$

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Montgomery's trick

Method	Cost	$I = 9M$
Naïve	$10\,(I + 2M + S + 8A) + 5A$	110M
Unified	$5\,(I + 4M + 2S + 14A)$	65M

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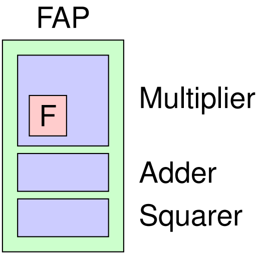
Unified	$5\,(I + 4M + 2S + 14A)$	65M
Unified + Montgomery	$I + 17M + 2S + 9A + 5\,(4M + 2S + 14A)$	46M

- Trades inversions to multiplications
- $1/x_1$ and $1/x_2$ computed so that $1/x_1 = x_2/(x_1 x_2)$ and $1/x_2 = x_1/(x_1 x_2)$
- n inversions computed with $3(n-1)$ multiplications and 1 inversion

Architecture



Massey-Omura multiplier

- Bit-serial, only one F-block
- Latency: $m + c + 1$ clock cycles

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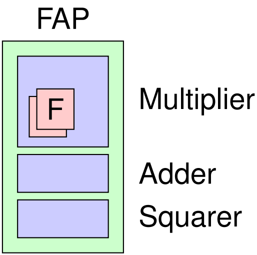

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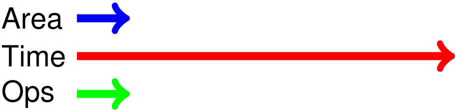

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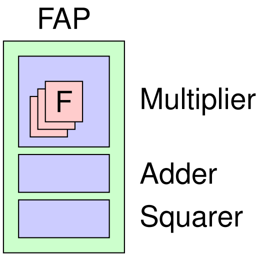

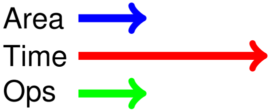

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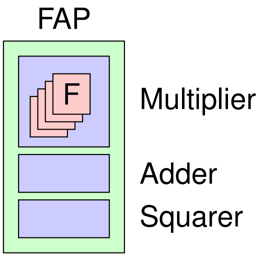

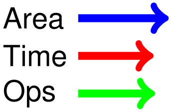

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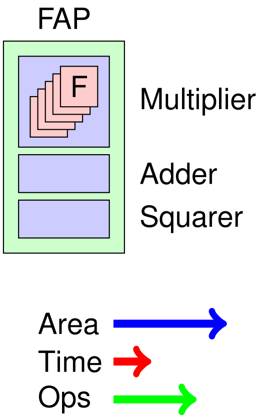

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- Latency: $\lceil \frac{m}{\nu} \rceil + c + 1$
- ν should be from the set $\mathcal{F} : \{1 - 15, 17, 19, 21, 24, 28, 33, 41, 55, 82, 163\}$

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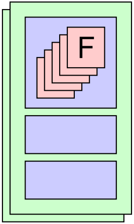

Massey-Omura multiplier

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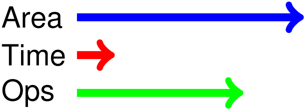

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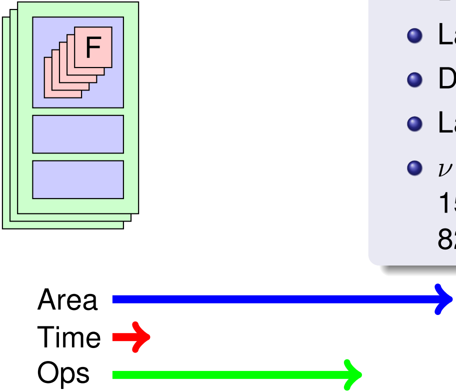

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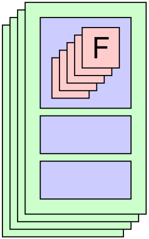

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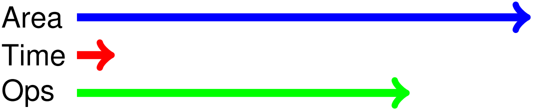

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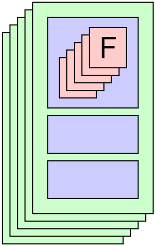

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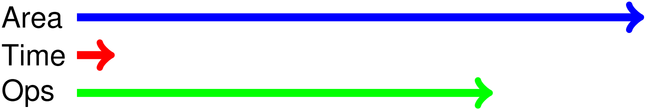

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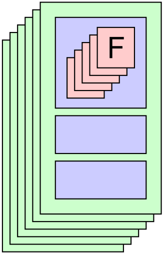

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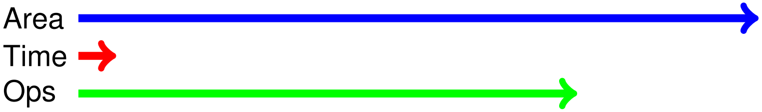

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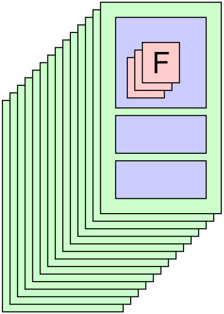

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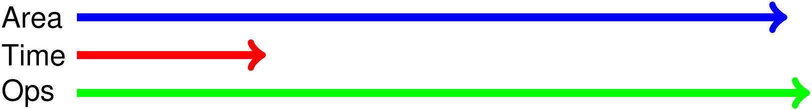
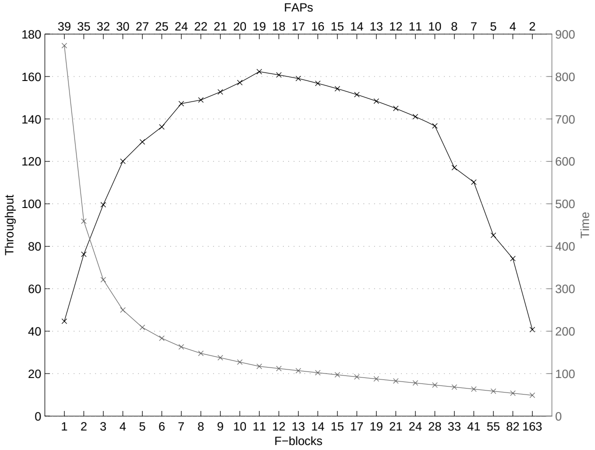


Parameters


FAPs
39 35 32 30 27 25 24 22 21 20 19 18 17 16 15 14 13 12 11 10 8 7 5 4 2
Throughput
0 20 40 60 80 100 120 140 160 180
Time
0 100 200 300 400 500 600 700 800 900
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 17 19 21 24 28 33 41 55 82 163
F−blocks

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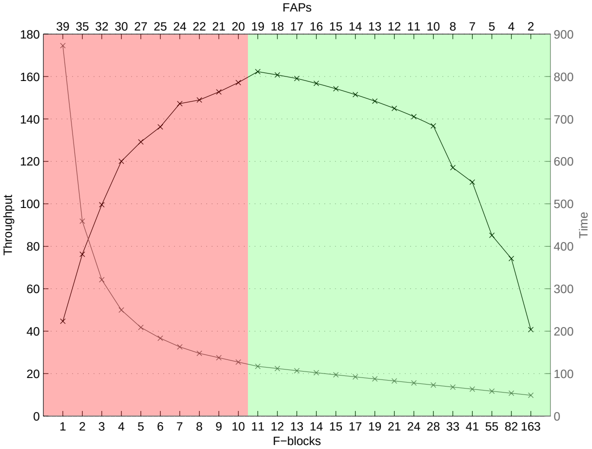
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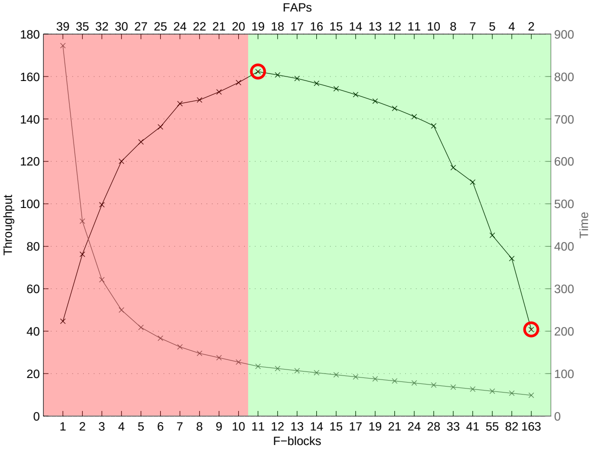
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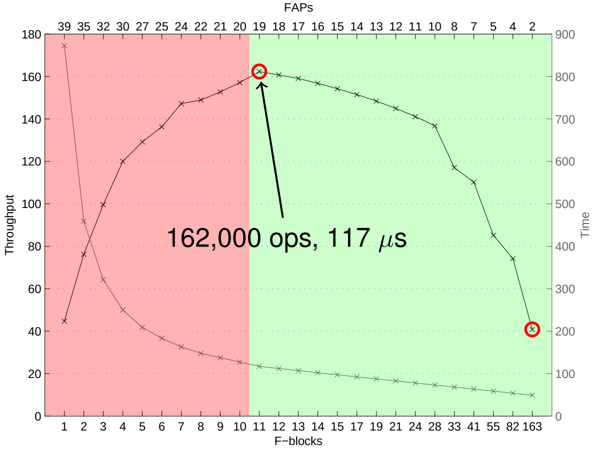
FAPs
39 35 32 30 27 25 24 22 21 20 19 18 17 16 15 14 13 12 11 10 8 7 5 4 2
Throughput
0 20 40 60 80 100 120 140 160 180
Time
0 100 200 300 400 500 600 700 800 900
162,000 ops, 117 µs
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 17 19 21 24 28 33 41 55 82 163
F−blocks

Results on an Altera Stratix II S180C3

- VHDL
- Altera Quartus II 6.0 SP1

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- 240 M512 (26 %), 305 M4K (40 %)
- Two clocks: 164 MHz and 82 MHz

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Performance

- One verification 114.2 μs (average)
- Up to 166,000 ops!

Conclusions and future work

- Very high ops achievable with modern FPGAs
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  - Development in FPGAs: speed and area
  - Parallelization
  - Time of single operation vs. ops
- Future work:
  - Polynomial basis?
  - Counterpart implementations for signature generation
  - Other operations (hash, modular arithmetic)
  - Possible problems (side channel attacks, power, etc.)

Thank you.
Questions?