

CURRICULUM VITAE

- Name:** Keijo Heljanko
- Date of Birth:** 7th Dec, 1971
- Nationality:** Finnish
- Marital Status:** Married, one child
- Office address:** Aalto University
School of Science and Technology
Department of Information and Computer Science
P.O. Box 15400, FI-00076 Aalto, Finland
Email: Keijo.Heljanko@tkk.fi
Homepage: <http://users.ics.tkk.fi/kepa>
Phone: +358-9-47025134
Fax: +358-9-47023369
- Language skills:** Finnish (mother tongue), English (excellent), German (satisfactory), Swedish (satisfactory)
- Education:** Doctor of Science (Technology), Department of Computer Science and Engineering, Helsinki University of Technology, Apr 2002.
Licentiate of Science (Technology), Department of Computer Science and Engineering, Helsinki University of Technology, Dec 1999.
Master of Science (Technology), Department of Computer Science and Engineering, Helsinki University of Technology, Sep 1997.
- Present Position:** Aug 2008 – (Jul 2013): Professor in Computer Science (Distributed Computation) at Department of Information and Computer Science, School of Science and Technology, Aalto University.
- Academic Career:** Aug 2005 – Jul 2008: Academy Research Fellow, Academy of Finland.
Jan 2003 – Jul 2008: Teaching Researcher, Department of Information and Computer Science, Helsinki University of Technology. (On leave Apr 2003 – Mar 2004 and Sep 2004 – Jul 2008.)
Jan 2006 – : Docent (Adjunct Professor) in Model Checking, Department of Information and Computer Science, Helsinki University of Technology.
Sep 2004 – Jul 2005: Academy Research Fellow (acting), Academy of Finland.
Apr 2003 – Mar 2004 Postdoctoral researcher (Wissenschaftlicher Mitarbeiter), Institute for Formal Methods in Computer Science, Software Security and Reliability Group (Prof. Javier Esparza), University of Stuttgart.
Jun 2002 – Dec 2002: Researcher, Laboratory for Theoretical Computer Science, Helsinki University of Technology.

Jan 2002 – May 2002: Project Manager, Laboratory for Theoretical Computer Science, Helsinki University of Technology.

Jan 2001 – Dec 2002: Senior Assistant, Laboratory for Theoretical Computer Science, Helsinki University of Technology. (On leave Jan 2001–Dec 2002.)

Sep 1997 – Dec 2001: Researcher, Laboratory for Theoretical Computer Science, Helsinki University of Technology.

Dec 1995 – Aug 1997: Research Assistant, Laboratory for Theoretical Computer Science, Helsinki University of Technology.

Publications:

Books

Esparza, J. and Heljanko, K.: *Unfoldings – A Partial-Order Approach to Model Checking*. EATCS Monographs in Theoretical Computer Science, ISBN: 978-3-540-77425-9, Springer, 172 p., 2008. Book homepage: <http://www.springer.com/978-3-540-77425-9>

Journals

Biere, A., Heljanko, K., Junttila, T., Latvala, T., and Schuppan V.: Linear Encodings of Bounded LTL Model Checking. *Logical Methods in Computer Science* 2(5:5):1–64, 2006. (doi: 10.2168/LMCS-2(5:5)2006).

Rintanen, J., Heljanko, K., and Niemelä, I.: Planning as Satisfiability: Parallel Plans and Algorithms for Plan Search. *Artificial Intelligence*, 170(12-13):1031–1080, Elsevier, 2006.

Jussila, T., Heljanko, K., and Niemelä, I.: BMC via On-the-Fly Determinization. *STTT - International Journal on Software Tools for Technology Transfer*, 7(2):89–101, Springer, 2005.

Heljanko, K. and Niemelä, I.: Bounded LTL Model Checking with Stable Models. *Theory and Practice of Logic Programming*, 3(4&5):519–550, Cambridge University Press, 2003.

Tauriainen, H. and Heljanko, K.: Testing LTL Formula Translation into Büchi Automata. *STTT - International Journal on Software Tools for Technology Transfer*, 4(1):57–70, Springer, 2002.

Latvala, T. and Heljanko, K.: Coping with Strong Fairness. *Fundamenta Informaticae*, 43(1-4):175–193, IOS Press, 2000.

Heljanko, K.: Using Logic Programs with Stable Model Semantics to Solve Deadlock and Reachability Problems for 1-Safe Petri Nets. *Fundamenta Informaticae*, 37(3):247–268, IOS Press, 1999.

Refereed Conferences and Workshops

Wieringa, S., Niemenmaa, M., Heljanko, K.: Tarmo: A Framework for Parallelized Bounded Model Checking. In *Proceedings of the 8th International Workshop on Parallel and Distributed Methods in Verification (PDMC'09)*, Electronic Proceedings in Theoretical Computer Science (EPTCS) 14, pp. 62–76, 2009.

Kähkönen, K., Lampinen, J., Heljanko, K., and Niemelä, I.: The LIME Interface Specification Language and Runtime Monitoring Tool. In *Proceedings of the 9th International Workshop on Runtime Verification (RV'2009)*, Lecture Note in Computer Science 5779, Springer, Grenoble, France, June 2009, pp. 93–100.

Axelsson, R., Heljanko, K., and Lange, M.: Analyzing Context-Free Grammars Using an Incremental SAT Solver. In *Proceedings of the 35th International Colloquium on Automata, Languages, and Programming (ICALP 2008), Part II*, Lecture Notes in Computer Science 5126, Springer, Reykjavik, Iceland, July 2008, pp. 410–422.

Dubrovin, J., Junttila, T., and Heljanko, K.: Symbolic Step Encodings for Object Based Communicating State Machines. In *Proceedings of the 10th IFIP International Conference on Formal Methods for Open Object-based Distributed Systems (FMOODS'2008)*, Lecture Notes in Computer Science 5051, Springer, Oslo, Norway, June 2008, pp. 96–112.

Heljanko, K., Junttila, T., Keinänen, M., Lange, M., and Latvala, T.: Bounded Model Checking for Weak Alternating Büchi Automata. In *Proceedings of the 18th International Conference on Computer Aided Verification (CAV'2006)*, Lecture Notes in Computer Science 4144, Springer, Seattle, USA, August 2006, pp. 95–108.

Heljanko, K., Junttila, T., and Latvala, T.: Incremental and Complete Bounded Model Checking for Full PLTL. In *Proceedings of the 17th International Conference on Computer Aided Verification (CAV'2005)*, Lecture Notes in Computer Science 3576, Springer, Edinburgh, Scotland, United Kingdom, July 2005. pp. 98–111.

Heljanko, K. and Ștefănescu, A.: Complexity Results for Checking Distributed Implementability. In *Proceedings of the 5th International Conference on Application of Concurrency to System Design (ACSD'2005)*, IEEE Computer Society Press, St Malo, France, June 2005. pp. 78–87.

Latvala, T., Biere, A., Heljanko, K., and Junttila, T.: Simple is Better: Efficient Bounded Model Checking for Past LTL. In *Proceedings of the 6th International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI'2005)*, Lecture Notes in Computer Science 3385, Springer, Paris, France, January 2005. pp. 380–395.

Latvala, T., Biere, A., Heljanko, K., and Junttila, T.: Simple Bounded LTL Model Checking. In *Proceedings of the 5th International Conference on*

Formal Methods in Computer-Aided Design (FMCAD'2004), Lecture Notes in Computer Science 3312, Springer, Austin, Texas, USA, November 2004. pp. 186–200.

Rintanen, J., Heljanko, K., and Niemelä, I.: Parallel Encodings of Classical Planning as Satisfiability. In *Proceedings of the 9th European Conference on Logics in Artificial Intelligence (JELIA'04)*, Lecture Notes in Computer Science 3229, Springer, Lisbon, Portugal, September 2004. pp. 307–319.

Jussila, T., Heljanko, K., and Niemelä, I.: BMC via On-the-Fly Determinization. In *Proceedings of the First International Workshop on Bounded Model Checking (BMC'2003)*, volume 89(4) of Electronic Notes in Theoretical Computer Science, Elsevier, Boulder, Colorado, USA, July 2003.

Pyhälä, T. and Heljanko, K.: Specification Coverage Aided Test Selection. In *Proceeding of the 3rd International Conference on Application of Concurrency to System Design (ACSD'2003)*, IEEE Computer Society, Guimaraes, Portugal, June 2003, pp. 187–195.

Heljanko, K., Khomenko, V., and Koutny, M.: Parallelisation of the Petri Net Unfolding Algorithm. In *Proceedings of the 8th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS'2002)*, Lecture Notes in Computer Science 2280, Springer, Grenoble, France, April 2002. pp. 371–385.

Heljanko, K. and Niemelä, I.: Bounded LTL Model Checking with Stable Models. In *Proceedings of the 6th International Conference on Logic Programming and Nonmonotonic Reasoning (LPNMR'2001)*, Lecture Notes in Artificial Intelligence 2173, Springer, Vienna, Austria, September 2001, pp. 200–212.

Heljanko, K.: Bounded Reachability Checking with Process Semantics. In *Proceedings of the 12th International Conference on Concurrency Theory (Concur'2001)*, Lecture Notes in Computer Science 2154, Springer, Aalborg, Denmark, August 2001, pp. 218–232.

Esparza, J. and Heljanko, K.: Implementing LTL Model Checking with Net Unfoldings, In *Proceedings of the 8th International SPIN Workshop on Model Checking of Software (SPIN'2001)*, Lecture Notes in Computer Science 2057, Springer, Toronto, Canada, May 2001, pp. 37–56.

Heljanko, K. and Niemelä, I.: Answer Set Programming and Bounded Model Checking. In *Proceedings of the AAAI Spring 2001 Symposium on Answer Set Programming: Towards Efficient and Scalable Knowledge Representation and Reasoning*, AAAI Press, Technical Report SS-01-01, Stanford, USA, March 2001, pp. 90–96.

Tauriainen, H. and Heljanko, K.: Testing SPIN's LTL Formula Conversion into Büchi Automata with Randomly Generated Input. In *Proceedings of the 7th International SPIN Workshop on Model Checking of Software*

(*SPIN'2000*), Lecture Notes in Computer Science 1885, Springer, Stanford University, California, USA, August 2000, pp. 54–72.

Heljanko, K.: Model Checking with Finite Complete Prefixes is PSPACE-complete. In *Proceedings of the 11th International Conference on Concurrency Theory (Concur'2000)*, Lecture Notes in Computer Science 1877, Springer, State College, Pennsylvania, USA, August 2000, pp. 108–122.

Esparza, J. and Heljanko, K.: A New Unfolding Approach to LTL Model Checking. In *Proceedings of the 27th International Colloquium on Automata, Languages and Programming (ICALP'2000)*, Lecture Notes in Computer Science 1853, Springer, Geneva, Switzerland, July 2000, pp. 475–486.

Heljanko, K.: Using Logic Programs with Stable Model Semantics to Solve Deadlock and Reachability Problems for 1-Safe Petri Nets. In *Proceedings of Fifth International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS'99)*, Lecture Notes in Computer Science 1579, Springer, Berlin, March 1999, pp. 240–254.

Heljanko, K.: Minimizing Finite Complete Prefixes. In *Proceedings of the Workshop Concurrency, Specification & Programming 1999*, Warsaw University, Warsaw, Poland, September 1999, pp. 83–95.

Latvala, T. and Heljanko, K.: Coping With Strong Fairness – On-the-fly Emptiness Checking for Streett Automata. In *Proceedings of the Workshop Concurrency, Specification & Programming 1999*, Warsaw University, Warsaw, Poland, September 1999, pp. 107–118.

Heljanko, K.: Deadlock Checking for Complete Finite Prefixes Using Logic Programs with Stable Model Semantics (Extended Abstract). In *Proceedings of the Workshop Concurrency, Specification & Programming 1998*, Informatik-Bericht Nr. 110, Humboldt-University, Berlin, September 1998, pp. 106–115.

Varpaaniemi, K., Heljanko, K., and Lilius, J.: PROD 3.2 - An Advanced Tool for Efficient Reachability Analysis. In *Proceedings of the 9th International Conference on Computer Aided Verification (CAV'97)*, Lecture Notes in Computer Science 1254, Springer, Haifa, Israel, June 1997, pp. 472–475.

Heljanko, K.: Implementing a CTL Model Checker. In *Proceedings of the Workshop Concurrency, Specification & Programming 1996*, Informatik-Bericht Nr. 69, Humboldt-University, Berlin, September 1996, pp. 75–84.

Theses

Heljanko, K.: Combining Symbolic and Partial Order Methods for Model Checking 1-Safe Petri Nets. Research Report A71, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Finland, Feb 2002, 55 + 97p. D.Sc. (Tech.) Thesis.

Heljanko, K.: Deadlock and Reachability Checking with Finite Complete Prefixes. Research Report A56, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Dec 1999, 70p. Licentiate's Thesis.

Heljanko, K.: Model Checking the Branching Time Temporal Logic CTL. Research Report A45, Digital Systems Laboratory, Helsinki University of Technology, Espoo, May 1997, 69p. Master's Thesis.

Technical Reports and Other Non-Refereed Scientific Publications

Jani Lampinen, Sami Liedes, Kari Kähkönen, Janne Kauttio, and Keijo Heljanko. Interface specification methods for software components. Technical Report TTK-ICS-R25, Helsinki University of Technology, Department of Information and Computer Science, Espoo, Finland, December 2009, 52p.

Kim Björkman, Juho Frits, Janne Valkonen, Jussi Lahtinen, Keijo Heljanko, Ilkka Niemelä, and Jari J. Hämäläinen. Verification of safety logic designs by model checking. In *Sixth American Nuclear Society International Topical Meeting on Nuclear Plant Instrumentation, Control, and Human-Machine Interface Technologies NPIC&HMIT*, Knoxville, Tennessee, April 5-9, American Nuclear Society, LaGrande Park, IL, 2009, on CD-ROM.

Janne Valkonen, Matti Koskimies, Kim Björkman, Keijo Heljanko, Ilkka Niemelä, and Jari J. Hämäläinen. Formal Verification of Safety Automation Logic Designs. In *Automaatio XVIII Seminaari 2009*, 17-18.3.2009, Helsinki, Finnish Society of Automation, 2009.

Kim Björkman, Juho Frits, Janne Valkonen, Keijo Heljanko, and Ilkka Niemelä: Model-Based Analysis of a Stepwise Shutdown Logic - MODSAFE 2008 Work Report. VTT Working Papers 115, VTT Technical Research Centre of Finland, Espoo, Finland, Mar 2009, 41 p.

Valkonen, J., Koskimies, M., Pettersson, V., Heljanko, K., Holmberg, J.-E., Niemelä, I., and Hämäläinen, J. J.: Formal verification of safety I&C system designs: Two nuclear power plant related applications. In *Enlarged Halden Programme Group Meeting – Proceedings of the Man-Technology-Organisation Sessions*, page C4.2. Institutt for Energiteknikk, Halden, Norway, May 2008, 11 p.

Valkonen, J., Karanta, I., Koskimies, M., Heljanko, K., Niemelä, I., Sheridan, D., and Bloomfield, R. E.: NPP Safety Automation Systems Analysis – State of the Art. VTT Working Papers 94, VTT Technical Research Centre of Finland, Espoo, Finland, April 2008, 62 p.

Valkonen, J., Pettersson, V., Björkman, K., Holmberg, J., Koskimies, M., Heljanko, K., and Niemelä, I.: Model-Based Analysis of an Arc Protection and an Emergency Cooling System – MODSAFE 2007 Working Report. VTT Working Papers 93, VTT Technical Research Centre of Finland, Espoo, Finland, February 2008, 51 p.

Heljanko, K.: Verification Methods Based on Propositional Logic Satisfiability. Abstract in the Abstract collection of Finnish Mathematical Days 2008, Espoo, Finland, Jan 3-4, 1 p.

Dubrovin, J. and Junttila, T., and Heljanko, K.: Symbolic Step Encodings for Object Based Communicating State Machines. Technical Report B24, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Finland, December 2007, 25 p.

Rintanen, J., Heljanko, K., and Niemelä, I.: Planning as Satisfiability: Parallel Plans and Algorithms for Plan Search. Technical report 216, Institute of Computer Science at Freiburg University, 2005, 56p.

Heljanko, K. and Ştefănescu, A.: Complexity Results for Checking Distributed Implementability. Technical Report 05/2004, Institute of Formal Methods in Computer Science, University of Stuttgart, October 2004, 37p.

Latvala, T., Biere, A., Heljanko, K., and Junttila, T.: Simple Bounded LTL Model Checking. Research Report A92, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Finland, July 2004, 16p.

Rintanen, J., Heljanko, K., and Niemelä, I.: Parallel Encodings of Classical Planning as Satisfiability. Technical Report 198, Institute of Computer Science, Freiburg University, February 2004, 8p.

Heljanko, K., Khomenko, V., and Koutny, M.: Parallelisation of the Petri Net Unfolding Algorithm. Technical Report CS-TR-733, Department of Computing Science, University of Newcastle upon Tyne, June 2001, 14p.

Esparza, J. and Heljanko, K.: Implementing LTL Model Checking with Net Unfoldings, Research Report A68, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Finland, May 2001, 29p.

Heljanko, K. and Niemelä, I.: Petri Net Analysis and Nonmonotonic Reasoning. In *Leksa Notes in Computer Science - Festschrift in Honour of Professor Leo Ojala*, Research Report A63, Helsinki University of Technology, Laboratory for Theoretical Computer Science, October 2000, pp. 7–19.

Esparza, J. and Heljanko, K.: A New Unfolding Approach to LTL Model Checking. Research Report A60, Laboratory for Theoretical Computer Science, Helsinki University of Technology, Espoo, Finland, April 2000, 32p.

Grants:

Grant for research project “Computer Aided Verification Theory and Tools” led by Keijo Heljanko from Technology Industries of Finland Centennial Foundation (200 000 Euros total, project duration Jan 2007–Dec 2009), Nov 2006.

Grant for “Outstanding junior research group of Helsinki University of Technology (TKK)” to “Model Checking Research Group” led by Keijo Heljanko for the two year term Aug 2006–Jul 2008 (30000 Euros/year). Only three grants were granted at TKK.

Academy of Finland grant for research expenses of the Academy Research Fellow under the title “Testing, Verification, and Synthesis of Distributed Systems” for two years 2009-2010 (on average 50000 Euros/year, for funding a doctoral student), three years 2006-2008 (42800 Euros/year, for funding a doctoral student), 2005 (4000 Euros, for travel).

Academy of Finland grant for research work abroad, 2003.

Thesis Supervisor: Master’s Thesis: Tuomas Launiainen: *Model Checking PSL Safety Properties*. Helsinki University of Technology, Department of Information and Computer Science, Apr 2009.

Thesis Instructor: Doctoral Thesis: Misa Keinänen: *Techniques for Solving Boolean Equation Systems*, Helsinki University of Technology, Department of Computer Science and Engineering, Dec 2006.

Doctoral Thesis: Heikki Tauriainen: *Automata and Linear Temporal Logic: Translations with Transition-Based Acceptance*, Helsinki University of Technology, Department of Computer Science and Engineering, Oct 2006.

Doctoral Thesis: Toni Jussila: *On Bounded Model Checking of Asynchronous Systems*, Helsinki University of Technology, Department of Computer Science and Engineering, Oct 2005.

Doctoral Thesis: Timo Latvala: *Automata-Theoretic and Bounded Model Checking for Linear Temporal Logic*, Helsinki University of Technology, Department of Computer Science and Engineering, Aug 2005.

Licentiate’s Thesis: Heikki Tauriainen: *On the Translation of Linear Temporal Logic into Alternating and Nondeterministic Automata*. Helsinki University of Technology, Department of Computer Science and Engineering, Nov 2003.

Master’s Thesis: Kari Kähkönen: *Automated Dynamic Test Generation for Sequential Java Programs*. Helsinki University of Technology, Department of Information and Computer Science, Jul 2008.

Master’s Thesis: Jani Lampinen: *Interface specification methods for software components*. Helsinki University of Technology, Department of Information and Computer Science, Jun 2008.

Master’s Thesis: Jussi Lahtinen: *Model checking timed safety instrumented systems*. Helsinki University of Technology, Department of Information and Computer Science, Jun 2008.

Master’s Thesis: Matti Koskimies: *Applying model checking to analysing safety instrumented systems*. Helsinki University of Technology, Department of Information and Computer Science, Jun 2008.

Master’s Thesis: Jukka Honkola: *Modeling the SpaceWire Architecture with the Lyra Method*. Helsinki University of Technology, Department of Computer Science and Engineering, Mar 2006. Jointly instructed with M.Sc. Sari Leppänen of Nokia Research Center.

Master's Thesis: Topi Pohjolainen: *Model checking a client-server system with a scalable level of concurrency*. Helsinki University of Technology, Department of Electrical and Communications Engineering, May 2005.

Master's Thesis: Tuomo Pyhälä: *Specification-Based Test Selection in Formal Conformance Testing*. Helsinki University of Technology, Department of Computer Science and Engineering, Dec 2003.

Master's Thesis: Nikolaj Cancar: *Model Based Testing Using UML*. Helsinki University of Technology, Department of Electrical and Communications Engineering, Oct 2003.

Master's Thesis: Timo Latvala: *Model Checking Linear Temporal Logic Properties of Petri Nets with Fairness Constraints*. Helsinki University of Technology, Department of Electrical and Communications Engineering, Oct 2000.

Master's Thesis: Heikki Tauriainen: *Automated Testing of Büchi Automata Translators for Linear Temporal Logic*. Helsinki University of Technology, Department of Computer Science and Engineering, Oct 2000. (Selected as the best Master's Thesis on the area of Computer Science in the year 2000 by the Finnish Society for Computer Science.)

Thesis Opponent: Doctoral Thesis: Henri Hansen: *Alternatives to Büchi Automata*, Tampere University of Technology, Department of Information Technology, Oct 2007.

Thesis Reviewer: Doctoral Thesis Pre-examiner: Jukka Suomela: *Optimisation Problems in Wireless Sensor Networks: Local Algorithms and Local Graphs*. University of Helsinki, Department of Computer Science, Apr 2009.

Doctoral Thesis Pre-examiner: Pauli Miettinen: *Matrix Decomposition Methods for Data Mining: Computational Complexity and Algorithms*. University of Helsinki, Department of Computer Science Mar 2009.

Doctoral Thesis Pre-examiner: Henri Hansen: *Alternatives to Büchi Automata*, Tampere University of Technology, Department of Information Technology, Jun 2007.

Licentiate's Thesis: Emilia Oikarinen: *Modular Answer Set Programming*, Helsinki University of Technology, Department of Computer Science and Engineering, Nov 2006.

Licentiate's Thesis: Misa Keinänen: *Solving Boolean Equation Systems*. Helsinki University of Technology, Department of Computer Science and Engineering, Apr 2005.

Master's Thesis: Aleksi Hänninen: *Boolean Satisfiability Problem and Cryptography*, Helsinki University of Technology, Department of Information and Computer Science, Mar 2008.

Thesis Committee: Member of the doctoral Thesis examination committee of Doctoral Thesis: Noomene Ben Henda: *Infinite-state Stochastic and Parameterized Systems*, Uppsala University, Jun 2008.

- PC member:**
- The 9th International Workshop on Parallel and Distributed Methods in Verification (PDMC 2010).
 - The 10th International Conference on Application of Concurrency in System Design (ACSD 2010).
 - The 8th International Workshop on Parallel and Distributed Methods in Verification (PDMC 2009).
 - The 16th International Symposium on Temporal Representation and Reasoning (TIME 2009).
 - The 9th International Conference on Application of Concurrency in System Design (ACSD 2009).
 - 35th Conference on Current Trends in Theory and Practice of Computer Science (SOFSEM 2009), Track: Techniques and Tools for Formal Verification.
 - The 8th International Conference on Application of Concurrency in System Design (ACSD 2008).
 - The 7th International Workshop on Parallel and Distributed Methods in Verification (PDMC 2008).
 - The 7th International Conference on Application of Concurrency in System Design (ACSD 2007).
 - The 14th International Symposium on Temporal Representation and Reasoning (TIME 2007).
 - Workshop on unfolding and partial order techniques (UFO 2007).
 - The 13th International Symposium on Temporal Representation and Reasoning (TIME 2006).
- Tutorials:**
- Advanced Full Day Tutorial on Bounded Model Checking at the joint conference ACSD 2006/ATPN 2006 (jointly organised with Tommi Junttila), June 2006.
- Reviewing:**
- RPF, the Research Promotion Foundation (RPF) of Cyprus, Evaluator of a research project in computer science, 2009.
 - SNSF, Swiss National Science Foundation, Evaluator of research projects in computer science, 2009.
 - EU FP7, DG INFSO, Embedded Systems, Independent expert reviewer for a research project, 2009.
 - ARRS, the Slovenian Research Agency, Evaluator of research projects in computer science, 2009, 2008.
 - ARRS, the Slovenian Research Agency, Member of the evaluation panel for research programmes in computer science, 2008.
 - NWO, the Netherlands Organization for Scientific Research, review of a grant proposal, 2002.

WWTF, the Wiener Wissenschafts-, Forschungs- und Technologiefonds (Vienna Science and Technology Fund), review of a grant proposal, 2008.

Fundamenta Informaticae, 2009, 2003.

Software Testing, Verification and Reliability, 2009.

Theoretical Computer Science, 2009.

Acta Informatica, 2008.

Transactions on Petri Nets and Other Models of Concurrency (ToPNoC), 2008–2007.

IEEE Transactions on Automatic Control, 2008–2005.

Information Processing Letters (IPL), 2007, 2005.

IEEE Transactions on Computers, 2007.

Nordic Journal of Computing, 2006–2005.

Formal Methods in System Design, 2005.

Formal Methods Letters (FML), 2005.

Journal of Systems and Software (JSS), 2004.

International Journal of Foundations of Computer Science, 2003.

Software and System Modeling (SoSyM) Journal, 2003–2002.

The Computer Journal, 2002–2001.

In addition a reviewer for 45+ international conferences and workshops.

Positions of trust: European Science Foundation, Vice member of the Management Committee of Action IC0901: Rich-Model Toolkit - An Infrastructure for Reliable Computer Systems, 2009–

Member of the Steering Group of Computing Infrastructure for Computational Science at Faculty of Information and Natural Sciences, 2009–

Board of Helsinki Graduate School in Computer Science and Engineering (HeCSE), 2006–

Member of the Steering Group of Department of Information and Computer Science, 2008–

Research visits: One year postdoc position at University of Stuttgart (see Academic Career).
Technische Universität München, Institut für Informatik, Lehrstuhl VII (Theoretical Computer Science and Foundations of AI), Prof. W. Brauer and Prof. J. Esparza, 1999–2000 (8 months).

Research interests: Distributed computation, computer aided verification tools and algorithms, model checking, testing, synthesis, temporal logic, net unfoldings

References:

Prof. Ilkka Niemelä
Aalto University
School of Science and Technology
Department of Information and Computer Science
P.O. Box 15400
FI-00076 Aalto, Finland
Email: Ilkka.Niemela@tkk.fi
Phone: +358 9 47023290

Prof. Javier Esparza
Technische Universität München
Institut für Informatik (I7)
Boltzmannstraße 3
D-85748 Garching bei München, Germany
Email: esparza@in.tum.de
Phone: +49 89 289 17204