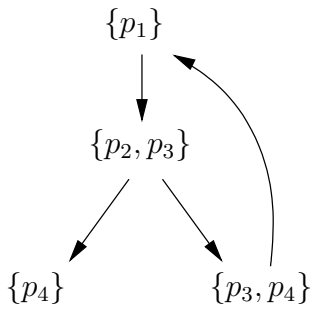
T–79.4301 **Autumn 2008**
Parallel and Distributed Systems
Tutorial 10 – Solutions

1. The reachability graph of the P/T net is shown below. The net is 1-bounded, meaning that at most one marker is at each state at any time. The states of the reachability graph are labelled as sets of places where a marker exists.



2. The state $\{p_4\}$ in the reachability graph has a deadlock, because it does not have any transitions enabled.

3. The following Promela program simulates the given P/T net. The `Place` type is defined as a boolean, since the P/T net is 1-bounded.

```
#define Place bool
Place p1, p2, p3, p4;

#define in1(x) (x>0) -> x--
#define in2(x,y) (x>0 && y>0) -> x--; y--
#define out1(x) x++
#define out2(x,y) x++; y++

init {
  atomic {p1=1; p2=0; p3=0; p4=0};
  do
  :: atomic { in1(p1) -> out2(p2,p3) }
  :: atomic { in2(p2,p3) -> out1(p4) }
  :: atomic { in1(p2) -> out1(p4) }
  :: atomic { in2(p3,p4) -> out1(p1) }
  od
}
```

4. The LTS $L = L_1 \parallel L_2 \parallel L_3 \parallel L_4$ has the same reachability graph as the P/T net. Each component LTS has two states: the upper represents the situation where the corresponding place in the P/T net has a marker, and the lower represents the situation where the place is empty.